

**METHOD AND APPARATUS FOR ELIMINATION OF PROLOG AND
EPILOG INSTRUCTIONS IN A VECTOR PROCESSOR**

ABSTRACT OF THE DISCLOSURE

5 A method and apparatus for the elimination of prolog and epilog instructions in a
vector processor. To eliminate the prolog, a functional unit of the vector processor
has at least one input for receiving an input data value tagged with a data validity tag
and an output for outputting an intermediate result tagged with a data validity tag.
The data validity tags indicate the validity of the data. Before a loop is executed, the
10 data validity tags are set to indicate that the associated data values are invalid. During
execution of the loop body a functional unit checks the validity of input data. If all of
the input data values are valid the functional operation is performed, the
corresponding data validity tag set to indicate that the result is valid. If any of the
input data values is invalid, the data validity tag of the result is set to indicate that the
15 result is invalid. To eliminate the epilog, an iteration counter is associated with each
sink unit of the vector processor. When a specified number of data values have been
produced by a particular sink, no more data values are produced by that sink. The
instructions for the pipelined loop body may be repeated, without alteration, to
eliminate prolog and epilog instructions.